**BİLGİSAYAR ORGANİZASYONU VE TASARIMI LABORATUVARI UYGULAMA RAPORU**

**UYGULAMA NO:** 1

**UYGULAMA TARİHİ:** 19 EKİM 2016

**GRUP NO:**  G8

**GRUP ÜYELERİ**

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1358130060 Gülçin Çelebi

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-- Description: s girişine göre 8 işlemden birini yapıyor a ve b yi kullanarak ve sonucu f ye yazıyor

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_SIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity alu is

port(

A,B:in std\_logic\_vector(3 downto 0);

S:in std\_logic\_vector(2 downto 0);

F:out std\_logic\_vector(3 downto 0));

end alu;

architecture Behavioral of alu is

begin

process(A,B,S)

begin

case S is

when "000" =>

F<="0000";

when "001" =>

F<=B-A;

when "010" =>

F<=A-B;

when "011" =>

F<=A+B;

when "100" =>

F<=A XOR B;

when "101"=>

F<=A OR B;

when "110"=>

f<=A AND B;

when "111" =>

F<="1111";

when OTHERS =>

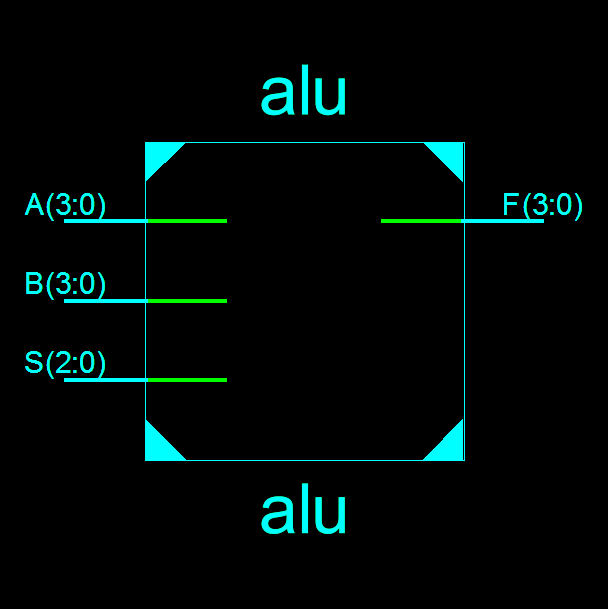
f<="1111";

end case;

end process;

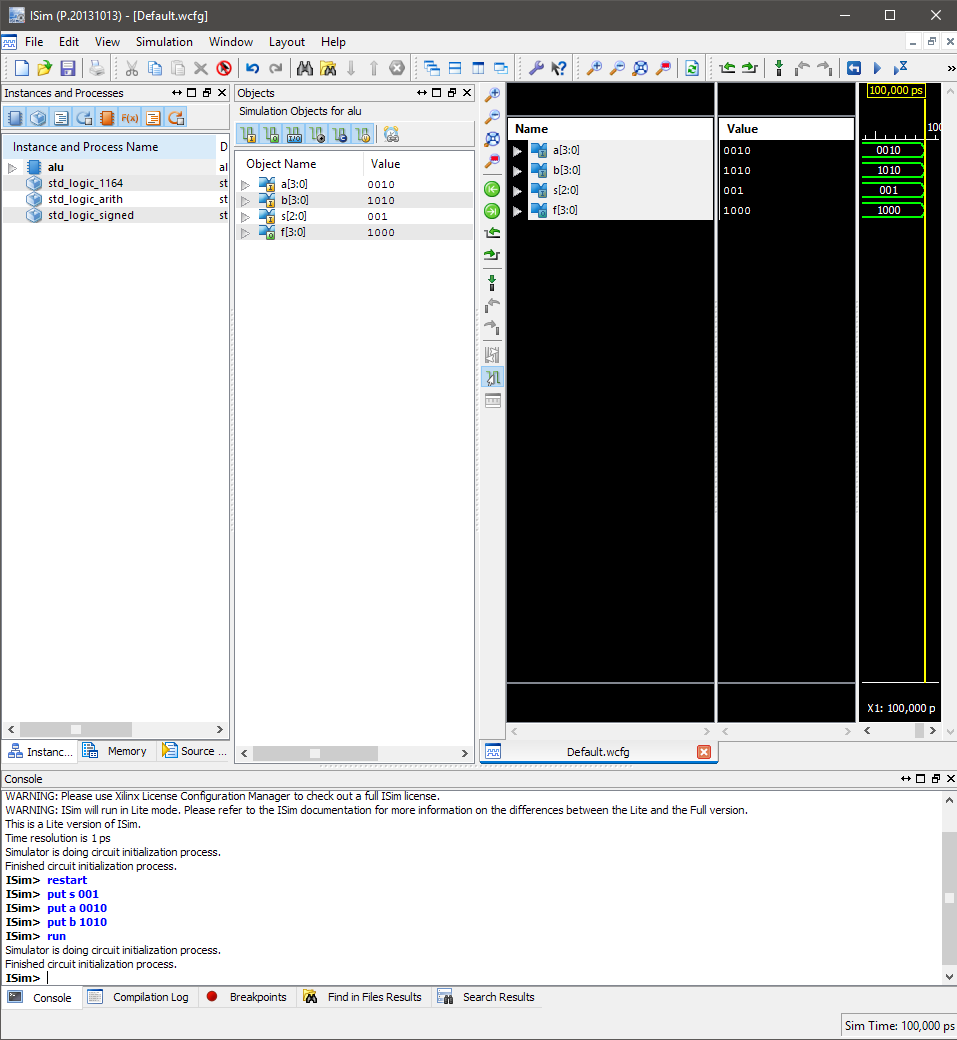
end Behavioral;

*Bölüm 2*



**RTL şeması**

*Bölüm 3*



**Waveform Diagram**